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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,526	06/23/2000	Joseph Herbst	108339-09031	1170

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EXAMINER	
LEVITAN, DMITRY	
ART UNIT	**PAPER NUMBER**
2662	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/599,526	HERBST, JOSEPH	
	Examiner	Art Unit	
	Dmitry Levitan	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15 and 22* is/are allowed.

6)☒ Claim(s) *1,5,8-14 and 16-21* is/are rejected.

7)☒ Claim(s) *2-4, 6 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Amendment, filed 03/09/05, has been entered. Claims 1-22 remain pending.

Claim Rejections - 35 USC § 112

Claims 11-12 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11 limitation "receiving a data storage/latch enable signal at a first input to the circuit/first flip-flop" is unclear, because it is not understood what "enable signal" is claimed. The disclosed circuit on Fig. 31 , comprising elements 101-103, has two inputs A and B, shown as data on Fig. 32. Examiner believes that data signals are not defined as "enable signal" and, in addition, the glitchless fractional clock pulse at the input of the storage unit 104 is disclosed as a data storage enable signal.

So Examiner does not understand, what is a data storage enable signal in the claimed circuit.

Claim Rejections - 35 USC § 103

1. Claims 1, 5, 8-10, 13, 14, 16-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nelson (US 4,756,010) in view of Kish (US 4,740,962).

2. Regarding claims 1, 5 and 8-10, Nelson substantially teaches the limitations of the claims:

A method and apparatus generating a glitchless fractional clock pulse in a circuit, wherein said glitchless fractional clock pulse is of shorter period than a system core clock pulse (data sample

pulses G compared with recovered clock F on Fig. 3A, generated by a circuit on Fig. 1 or 2 and 5:27-39, wherein the sample pulses are shorter than the recovered clock pulses).

Nelson does not teach transmitting glitchless fractional clock pulse from the circuit to a data storage element and storing data in the element upon receiving glitchless fractional clock pulse.

Kish teaches transmitting glitchless fractional clock pulse from the circuit to a data storage element and storing data in the element upon receiving glitchless fractional clock pulse (transmitting clock from the clock extractor 32 to the write clock input of FIFO 36 as shown on Fig. 3 and 4:12-24). It would have been obvious to one of ordinary skill in the art at the time the invention was made to add transmitting glitchless fractional clock pulse from the circuit to a data storage element and storing data in the element upon receiving glitchless fractional clock pulse of Kish to the system of Nelson to improve the system resistance to noise by utilizing data sampling in the center of the data signal (Nelson 7:36-40).

In addition, regarding claim 5, FIFO comprises numerous latches.

In addition, regarding claim 10, Nelson teaches receiving latch enable pulses (data sample pulses G on Fig. 3A).

3. Regarding claim 13, 17, 18 and 20, Nelson substantially teaches the limitations of the claim:

An apparatus generating a glitchless fractional clock pulse in a circuit, wherein said glitchless fractional clock pulse is of shorter period than a system core clock pulse (data sample pulses G compared with recovered clock F on Fig. 3A, generated by a circuit on Fig. 1 or 2 and 5:27-39),

having an activating input, a clock input and a logic output (circuit on Fig. 1 and 2 with POWER ON, RECOVERED CLOCK input F and DATA SAMPLE PULSES G) and data port interface (DATA INPUT A on Fig. 1).

Nelson does not teach one storage element having a data input, a storage enable input and data output.

Kish teaches one storage element having a data input, a storage enable input and data output (FIFO 36 comprising: data input DATA IN, write clock input 4:12-24 and DATA OUT on Fig. 3).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to connect the storage element of Kish to the system of Nelson to improve the system resistance to noise by utilizing data sampling in the center of the data signal (Nelson 7:36-40).

In addition, regarding claim 18, Nelson teaches a communication channel to deliver the data to the apparatus (radio channel 1:5-22).

4. Regarding claims 14 and 21, FIFO inherently comprises at least one latch, because latches are essential for the FIFO operation.

5. Regarding claim 19, Kish teaches memory management unit for controlling the storage of data (COUNTER 64 connected to FIFO 36 RESET input on Fig. 3).

6. Regarding claim 16, Nelson in view of Kish substantially teaches the limitation of the claim (see claim 13 rejection above).

Nelson in view of Kish does not teach generating the clock pulse at the logical output of the AND gate.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to add AND gate to the system of Nelson in view of Kish as a design choice, because NOR gate or other gates can work in the system as well (Nelson Fig. 1, NOR element 120).

Allowable Subject Matter

7. Claims 15 and 22 are allowed.

8. Claims 2-4, 6 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

9. Applicant's arguments filed 03/09/05 have been fully considered but they are not persuasive.

On page 14 of the Response, Applicant argues that receiving a data storage enable signal at first input to the circuit/flip-flop is not cited in claim11.

Examiner respectfully disagrees.

Examiner stated in the previous Office action, that the disclosed circuit on Fig. 31 , comprising elements 101-103, has two inputs A and B, shown as data on Fig. 32 and the input/data signals are not defined as "enable signal".

Claim 11 limitations are based on the structure of the same Fig. 32, so "enable signal" in this claim is as unclear as in claims 2, 3 and 6.

On page 21 of the Response, Applicant argues that Nelson does not teach generating a glitchless fractional clock pulse in a circuit, wherein said glitchless fractional clock pulse is of shorter period than a system core clock pulse.

Examiner respectfully disagrees.

Nelson teaches data sample pulses G compared with recovered clock F on Fig. 3A, generated by a circuit on Fig. 1 or 2 and 5:27-39, wherein the sample pulses are shorter than the recovered clock pulses. Examiner believes that interpretation of the recovered clock as core clock in the system of Nelson is reasonable, because the recovered clock is a core clock for the asynchronous receiver as disclosed in 1:5-44.

Examiner therefore believes that the cited references meet all the claims limitations and the rejection is proper.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dmitry Levitan whose telephone number is (571) 272-3093. The examiner can normally be reached on 8:30 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (571) 272-3088. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DL

Dmitry Levitan
Patent Examiner
04/20/05

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